

FIG. 2

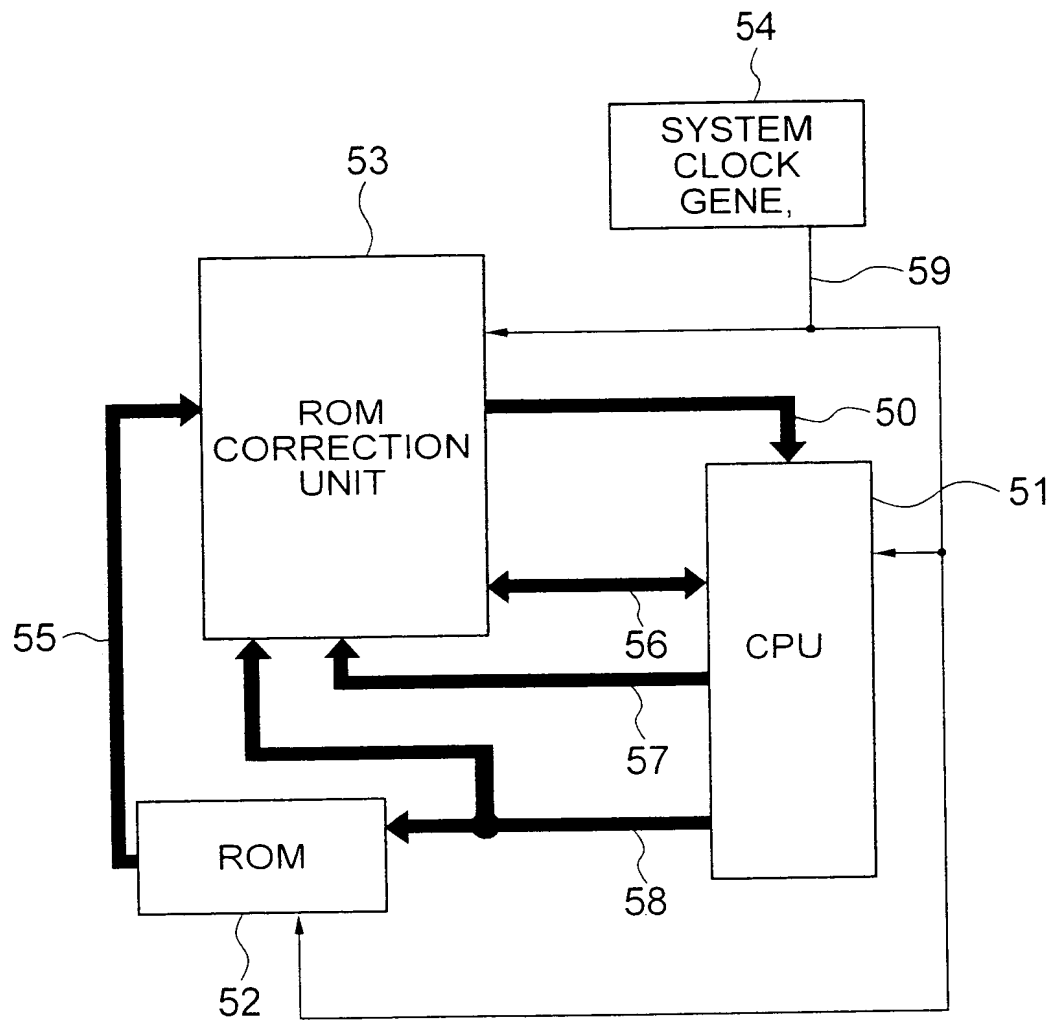


FIG. 3

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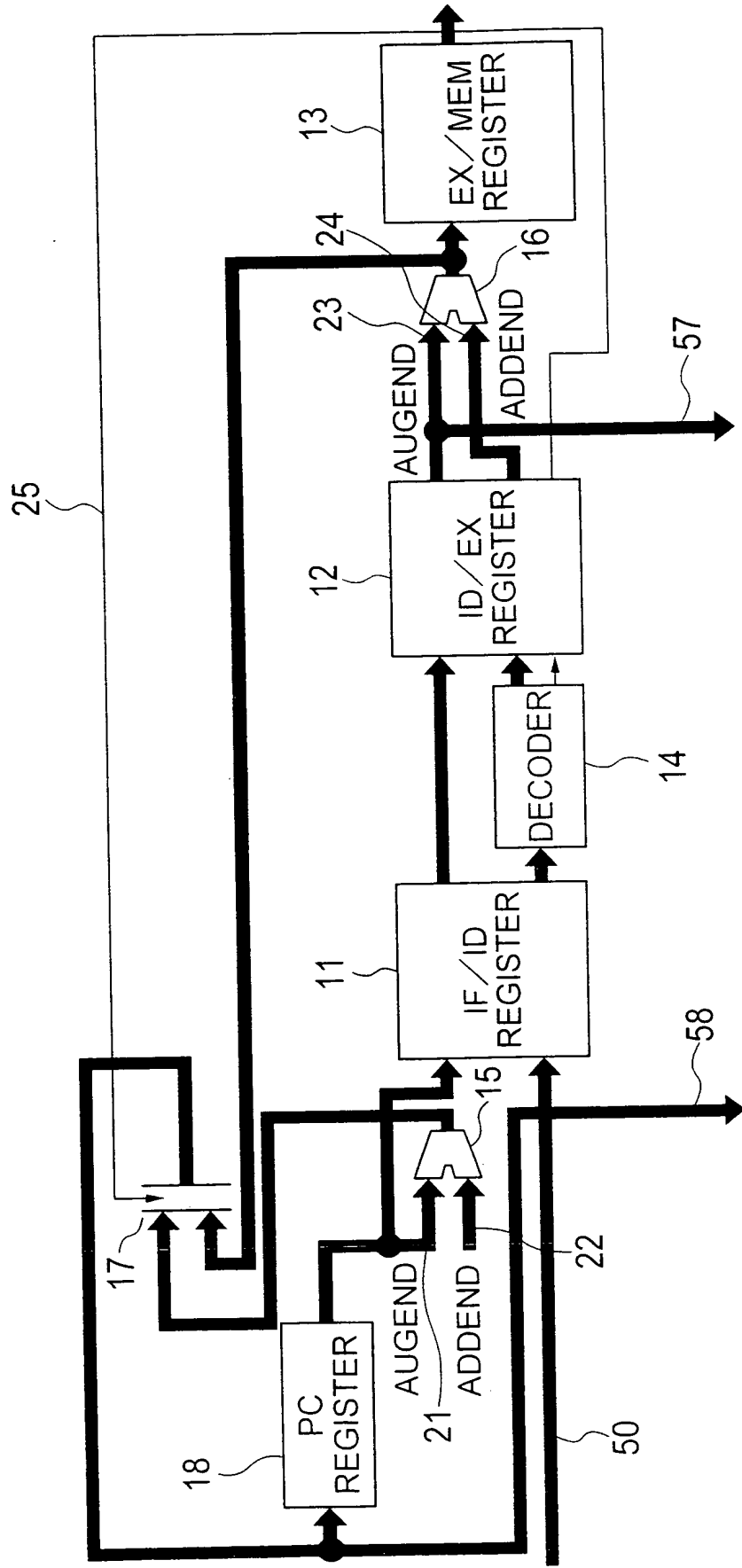


FIG. 4

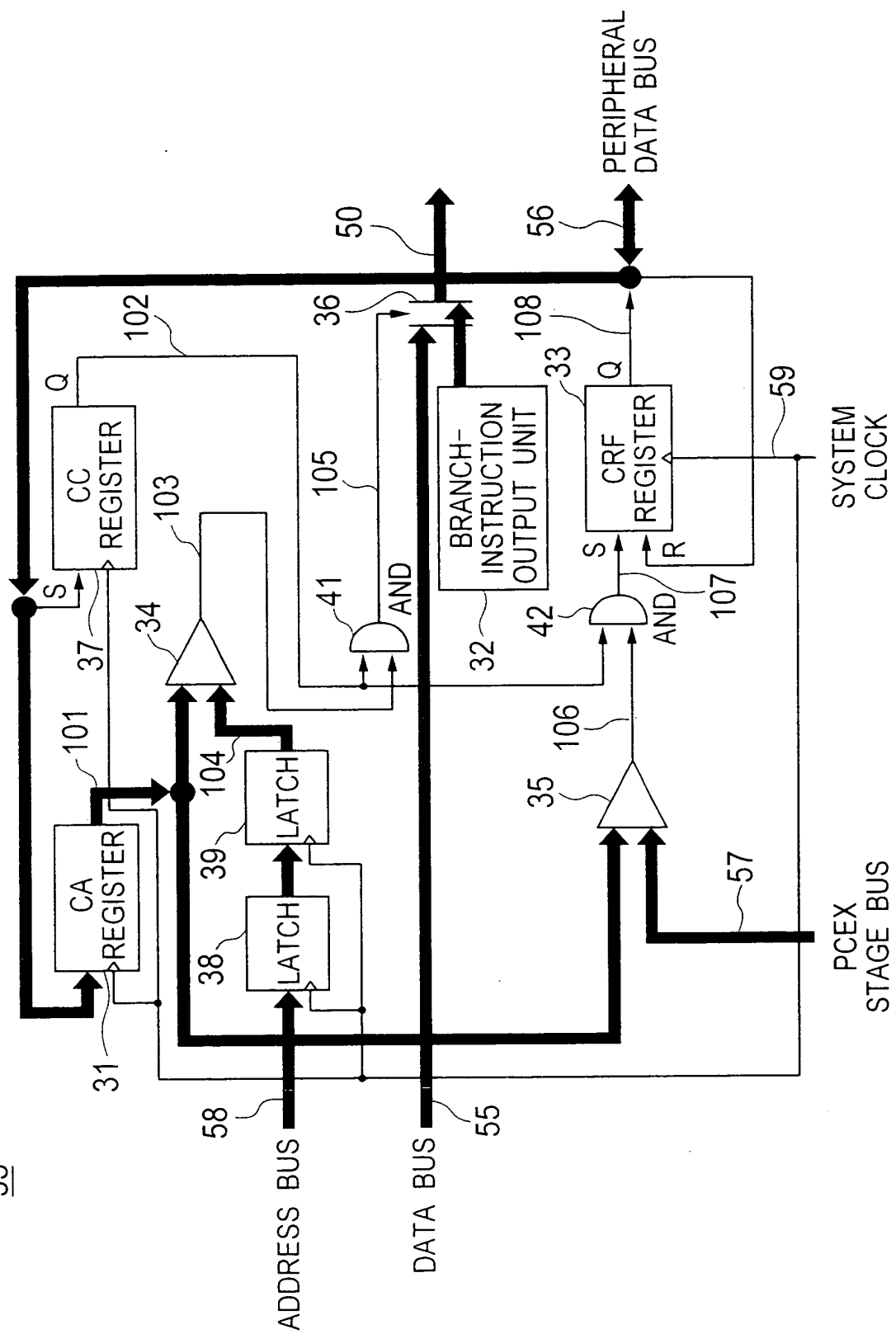


FIG. 5

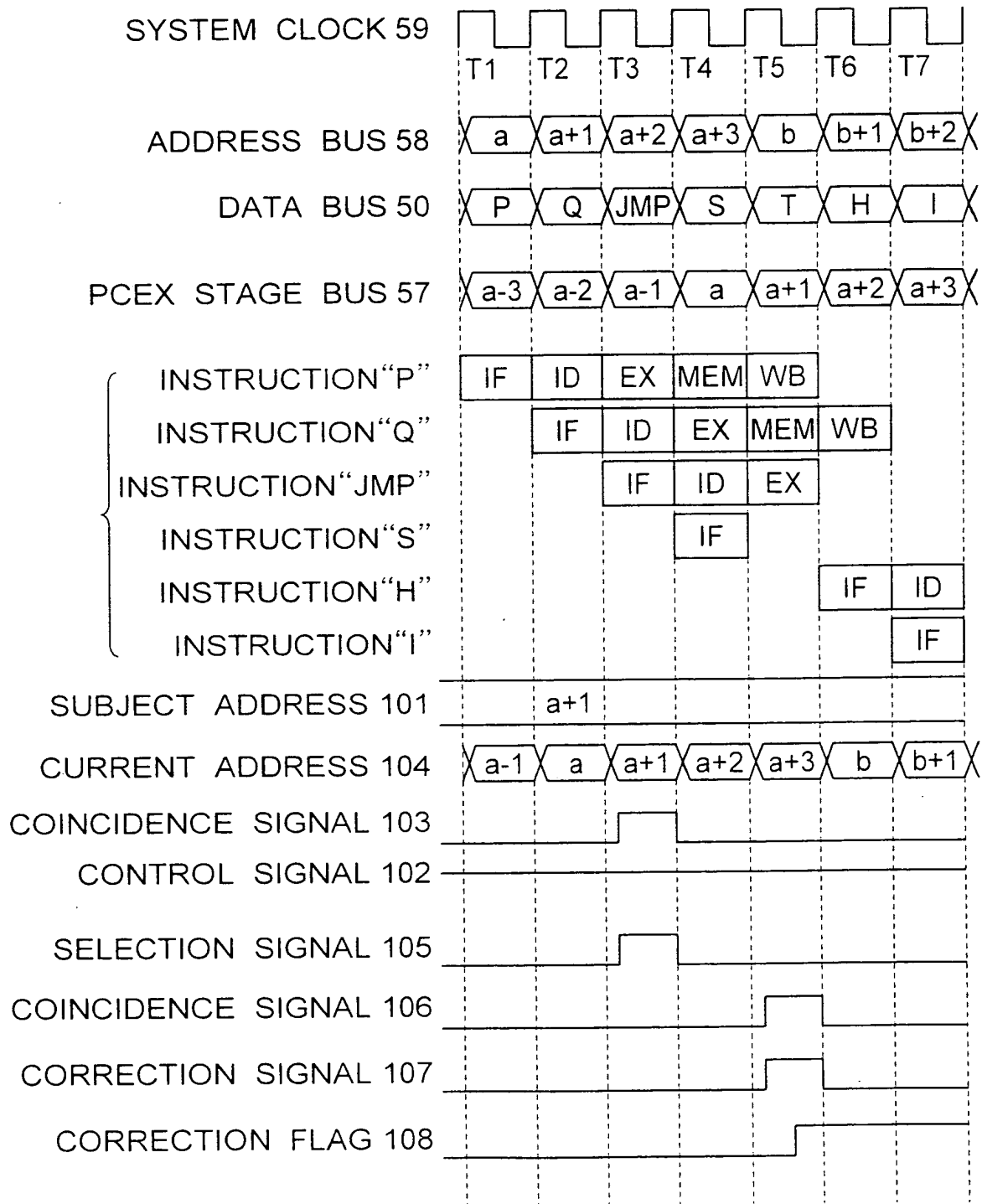


FIG. 6

ROM 53

ADDRESS	INSTRUCTION	
a-1	P	
a	Q	
a+1	R	SUBJECT ADDRESS
a+2	S	
a+3	T	
a+4	U	
}	}	
a+10	Z	RETURN ADDRESS
}	}	

FIG. 7

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ADDRESS	INSTRUCTION	
b	H	BRANCH ADDRESS
b+1	I	
b+2	J	
b+3	K	
}	}	
b+5	M	RETURN

FIG. 8

SYSTEM CLOCK	ADDRESS BUS	PC REGISTER	IF/ID REGISTER	ID/EX REGISTER	ADDER 16	
					OUTPUT	ADDEND 24
T2	a+1	a	a-1	a-2	a-2	0
T3	a+2	a+1	a	a-1	a-1	0
T4	a+3	a+2	a+1	a	a	0
T5	b	a+3	a+2	a+1	b	b-a-1
T6	b+1	b	a+3	a+2	a+2	0
T7	b+2	b+1	b	a+3	a+3	0
		ADDRESS ON IF STAGE	ADDRESS ON ID STAGE	ADDRESS ON EX STAGE		DIFFERENCE

FIG. 9

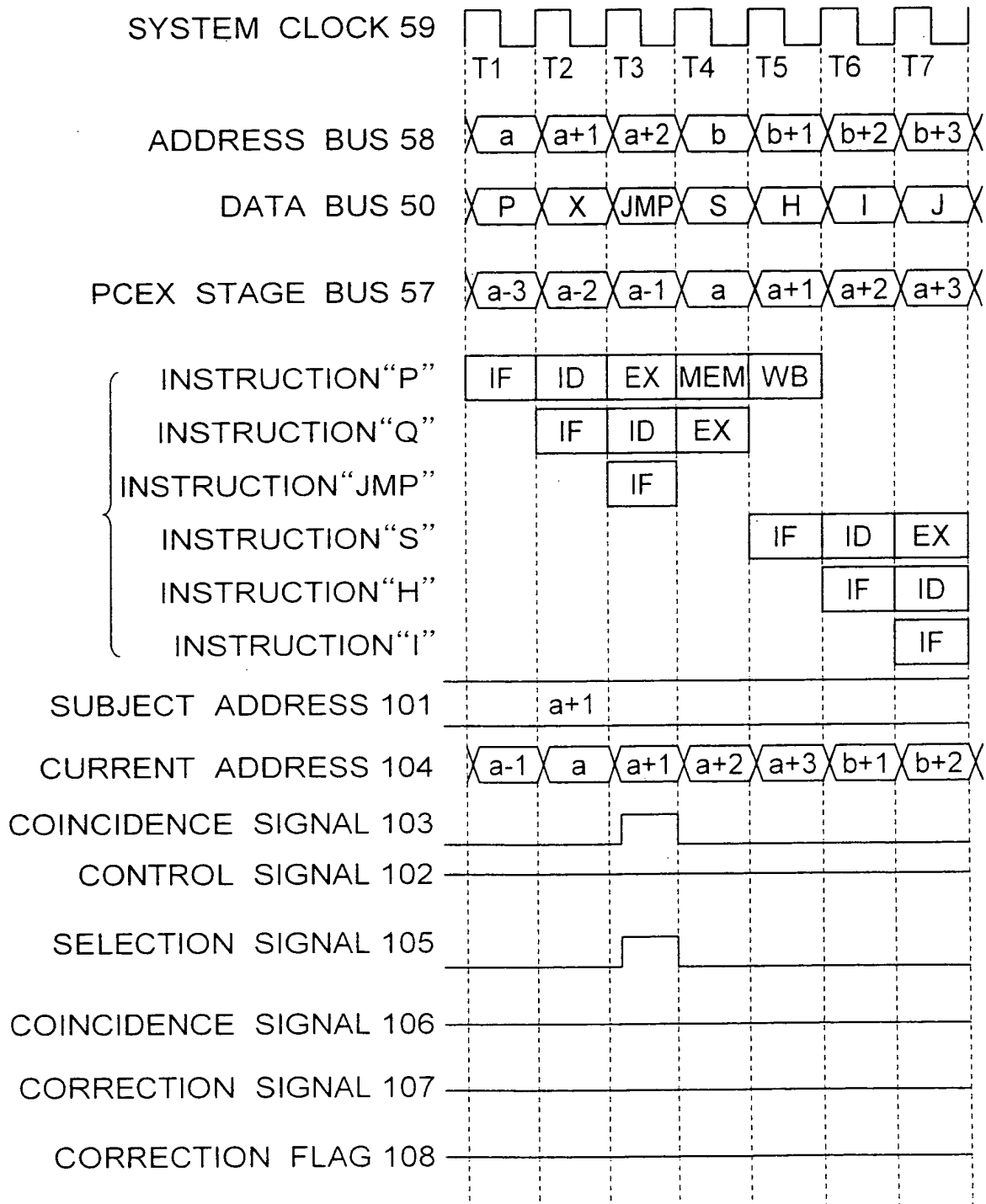


FIG. 10

ADDRESS	INSTRUCTION	
a-1	P	
a	X"JMP"	
a+1	R	SUBJECT ADDRESS
a+2	S	
a+3	T	
a+4	U	
}	}	
a+10	Z	RETURN ADDRESS
}	}	

FIG. 11

ADDRESS	INSTRUCTION	
b	H	BRANCH ADDRESS
b+1	I	
b+2	J	
b+3	K	
}	}	
b+5	M	RETURN

FIG. 12

SYSTEM CLOCK	ADDRESS BUS	PC REGISTER	IF/ID REGISTER	ID/EX REGISTER	ADDER 16	
					OUTPUT	ADDEND 24
T2	a+1	a	a-1	a-2	a-2	0
T3	a+2	a+1	a	a-1	a-1	0
T4	b	a+2	a+1	a	b	b-a
T5	b+1	b	a+2	a+1	a+1	0
T6	b+2	b+1	b	a+2	a+2	0
T7	b+3	b+2	b+1	b	b	0
		ADDRESS ON IF STAGE	ADDRESS ON ID STAGE	ADDRESS ON EX STAGE		DIFFERENCE

FIG. 13

